REMARKS

Claims 1-24 are presented for further examination. Claims 1, 8, 12, 13, 17, and 22 have been amended.

In the Office Action mailed January 8, 2009, the Examiner rejected claims 13-16 and 17-20 under 35 U.S.C. § 112, first paragraph, because the limitation of the identity signal transmitted on the single line was not supported. Claims 1-24 were rejected under 35 U.S.C. § 103(a) as unpatentable over previously-cited Curran in view of previously-cited Szepesi.

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

Section 112 Rejection

Independent claims 13 and 17 have been amended to eliminate the recitation of the identity signal being sent on the single line. In view of the foregoing amendment, applicants respectfully submit that claims 13 and 17, and corresponding dependent claims, are now in compliance with Section 112.

Section 103(a) Rejection

Applicants have amended the independent claims, which are claims 1, 8, 12, 13, 17, and 22 to now include the feature of the sorting pattern being compressed to $M \cdot \log_2 M$ bits, where M is a number of lines in the bus. Also included is a decompression of the selected sorting pattern received at a receiver on the bus. Support for this amendment is found beginning at page 9, line 5 through page 10, line 14 in which a compression module is described at the transmission end that compresses the bits of the sorting pattern on $M \cdot \log_2 M$ bits necessary for transmitting the sorting pattern on the number of lines, the compression module designated by reference number 3 in Figure 2. Reference number 4 designates a decompression module that at the reception end decompresses the $M \cdot \log_2 M$ bits for reconstructing the sorting pattern.

Curran describes a switching code that identifies the bus lines that are to be inverted, and it is a string as long as the number of bus lines: when a bit in the i-th position is "1," the corresponding bus line is to be complemented at the reception end to recover the

information transmitted. A 16-line bus has hence a switching code of the type "0001001011010011." In the present claimed invention, in contrast, the swapping pattern is a bit sequence that indicates the bus lines that are to be multiplexed, which is $M \cdot \log_2 M$ long, where M is the bus switch cluster depth. If N = 4, where N is the number of narrow busses, then the swapping pattern is eight bits long (see paragraph 55 of the published U.S. application). For example, a valid swapping pattern (namely a pattern that allows the transmitted information to be validly recovered at the reception end) is 0-2-3-1 (00101101 in binary). Not all the swapping patterns are valid. For example, 0-1-0-3 (00010011 in binary) does not allow the transmitted information to be validly recovered at the reception end. Finally, Szepesi discloses a clock signal merely used for clocking without any information content.

Applicants respectfully submit that all of the independent claims, *i.e.*, claims 1, 8, 12, 13, 17, and 22, are clearly allowable over the combination of Curran and Szepesi. The remaining corresponding dependent claims are allowable for the features recited therein as well as for the reasons why their corresponding independent claims are allowable.

In view of the foregoing, applicants respectfully submit that all of the claims in this application are now in condition for allowance. In the event the Examiner disagrees or finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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